TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

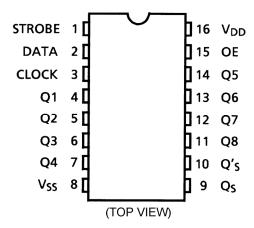
TC4094BP,TC4094BF,TC4094BFN

TC4094B 8-Stage Shift-and-Store Bus-Register

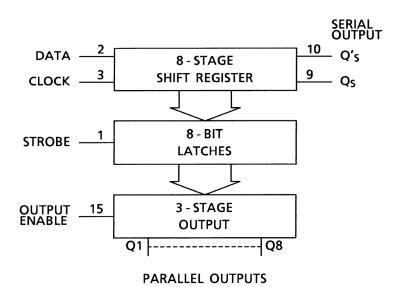
TC4094B is a SHIFT and STORE REGISTER that consists of an 8-bit shift register and an 8-bit latch. The read data in the shift register can be taken in the latch through the asynchronous STROBE input; therefore, the data transfer mode can hold output. And, since the parallel outputs is of 3-state construction, it can be directly connected to the 8-bit busline.

This register can be applied to Serial-to-parallel conversion, data receivers, etc.

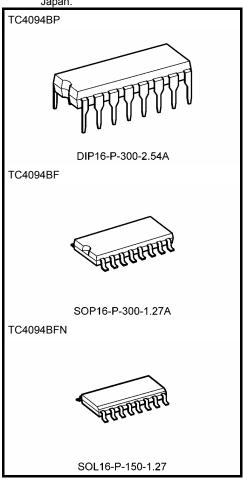
Pin Assignment



Block Diagram



Note: xxxFN (JEDEC SOP) is not available in



Weight

DIP16-P-300-2.54A : 1.00 g (typ.) SOP16-P-300-1.27A : 0.18 g (typ.) SOL16-P-150-1.27 : 0.13 g (typ.)

2007-10-01

Truth Table

CL	OE	ST	ר		PO	SO		
CL	_ OE ST D		D	Q1	Qn	Qs	Q's	
	Н	Н	L	L	Qn – 1	Q7	NC	
	Н	Н	Н	Н	Qn – 1	Q7	NC	
	Н	L	Х	NC	NC	Q7	NC	
	L	X	Х	HZ	HZ	Q7	NC	
$\overline{}$	Н	Х	Х	NC	NC	NC	Qs	
$\overline{}$	L	Х	Х	HZ	HZ	NC	Qs	

CL = Clock X = Don't care

OE = Output eneble NC = No change

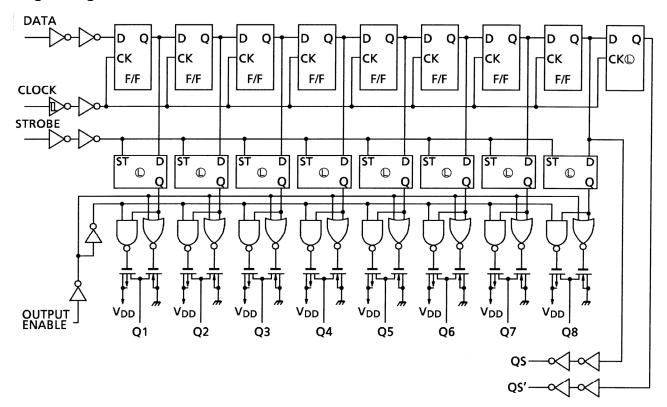
ST = Strobe HZ = High impedance

 $\mathsf{D} = \mathsf{Data}$

PO = Parallel outputs

SO = Serial outputs

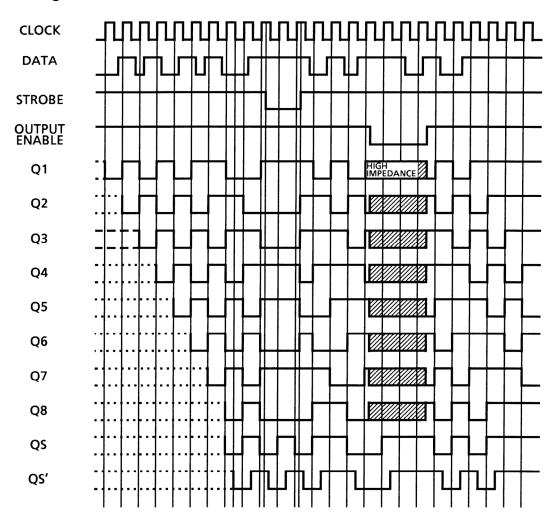
Logic Diagram



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LATCH

Timing Chart





Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
DC supply voltage	V_{DD}	V_{SS} – 0.5 to V_{SS} + 20	V
Input voltage	V _{IN}	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
Output voltage	V _{OUT}	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
DC input current	I _{IN}	±10	mA
Power dissipation	PD	300 (DIP)/180 (SOIC)	mW
Operating temperature range	T _{opr}	-40 to 85	°C
Storage temperature range	T _{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (V_{SS} = 0 V) (Note)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
DC supply voltage	V_{DD}	_	3	_	18	V
Input voltage	V _{IN}		0	_	V_{DD}	V

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Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{DD} or V_{SS} .



Static Electrical Characteristics ($V_{SS} = 0 V$)

Ob a manufaction		Sym-	Test Condition		-40)°C		25°C	5°C 85°		°C		
Charac	teristics	bol		V _{DD} (V)	Min	Max	Min	Тур.	Max	Min	Max	Unit	
			1.4.4	5	4.95	_	4.95	5.00	_	4.95	_		
High-level output voltage	V _{OH}	I _{OUT} < 1 μA	10	9.95	_	9.95	10.00	_	9.95	_	V		
i i i i i i i i i i i i i i i i i i i			$V_{IN} = V_{SS}, V_{DD}$	15	14.95	_	14.95	15.00	_	14.95	_		
			I _{OUT} < 1 μA	5	_	0.05	_	0.00	0.05	_	0.05		
Low-level voltage	output	V _{OL}	$V_{IN} = V_{SS}, V_{DD}$	10	_	0.05	_	0.00	0.05	_	0.05	V	
			VIN - VSS, VDD	15	_	0.05	_	0.00	0.05		0.05		
			V _{OH} = 4.6 V	5	-0.61		-0.51	-1.0	_	-0.42	_		
			V _{OH} = 2.5 V	5	-2.50	_	-2.10	-4.0	_	-1.70	_		
Output hig	h current	I _{OH}	V _{OH} = 9.5 V	10	-1.50	_	-1.30	-2.2	_	-1.10	_	mA	
			V _{OH} = 13.5 V	15	-4.00	_	-3.40	-9.0	_	-2.80	_		
			$V_{IN} = V_{SS}, V_{DD}$										
			V _{OL} = 0.4 V	5	0.61	_	0.51	1.2	_	0.42	_	mA	
Output lov	v current	l _{OL}	V _{OL} = 0.5 V	10	1.50	_	1.30	3.2	_	1.10	_		
Output lov	v current		V _{OL} = 1.5 V	15	4.00	_	3.40	12.0	_	2.80	_		
			$V_{IN} = V_{SS}, V_{DD}$										
		V _{IH}	V _{OUT} = 0.5 V, 4.5 V	5	3.5	_	3.5	2.75	_	3.5	_	V	
Input high	voltage		V _{OUT} = 1.0 V, 9.0 V	10	7.0	_	7.0	5.50	_	7.0	_		
input nign	voitage		V _{OUT} = 1.5 V, 13.5 V	15	11.0	_	11.0	8.25	_	11.0	_		
			$ I_{OUT} < 1 \mu A$										
			V _{OUT} = 0.5 V, 4.5 V	5		1.5	_	2.25	1.5	_	1.5		
Input low	voltage	V _{IL}	V _{OUT} = 1.0 V, 9.0 V	10	_	3.0	_	4.50	3.0	_	3.0	V	
input low	voltage	V IL	V _{OUT} = 1.5 V, 13.5 V	15	_	4.0	_	6.75	4.0	_	4.0	V	
	-		$ I_{OUT} < 1 \mu A$										
Input	"H" level	l _{IH}	V _{IH} = 18 V	18	_	0.1	_	10 ⁻⁵	0.1		1.0	μА	
current	"L" level	IJL	V _{IL} = 0 V	18		-0.1	_	-10^{-5}	-0.1		-1.0	μΛ	
3-state output	"H" level	I _{DH}	V _{out} = 18 V	18	_	0.4	_	10-4	0.4	_	12	μА	
leakage current	"L" level	I _{DL}	V _{out} = 0 V	18	_	-0.4	_	-10 ⁻⁴	-0.4	_	-12	μΑ	
Out to			$V_{IN} = V_{SS}, V_{DD}$	5	_	5	_	0.005	5	_	150		
Quiescent current	supply	I_{DD}	V _{IN} = V _{SS} , V _{DD} (Note)	10	_	10	_	0.010	10	_	300	μА	
			(Note)	15	_	20	_	0.015	20	_	600		

Note: All valid input combinations.



Dynamic Electrical Characteristics (Ta = 25°C, V_{SS} = 0 V, C_L = 50 pF)

		Test Condition		_	N4		
Characteristics	Symbol		V _{DD} (V)	Min	Тур.	Max	Unit
Output transition time			5	_	70	200	
(low to high)	t _{TLH}	_	10	_	35	100	ns
(low to riigir)			15	_	30	80	
Outrout transition time			5	_	70	200	
Output transition time	t _{THL}	_	10	_	35	100	ns
(high to low)			15	_	30	80	
Description delections			5	_	150	600	
Propagation delay time	t _{pLH}	_	10	_	75	250	ns
(CLOCK-Q _S)	t _{pHL}		15	_	55	190	
			5	_	155	460	
Propagation delay time	t _{pLH}	_	10	_	75	220	ns
(CLOCK-Q _S ')	t _{pHL}		15	_	55	150	
			5	_	190	840	
Propagation delay time	t _{pLH}	_	10	_	90	390	ns
(CLOCK-Q _n)	t _{pHL}		15	_	65	270	
			5	_	150	580	
Propagation delay time	t _{pLH}	_	10	_	70	290	ns
(STROBE-Q _n)	t _{pHL}		15	_	50	200	
			5	_	60	200	
Three state disable time	t _{PHZ}	$R_L = 1 \text{ k}\Omega$	10	_	35	100	ns
(OUTPUT ENABLE-Q _n)	^t PZH		15	_	30	80	
			5		70	200	
Three state disable time	tPLZ	$R_L = 1 \text{ k}\Omega$	10	_	40	100	ns
(OUTPUT ENABLE-Q _n)	tpzL		15	_	35	80	
			5		45	200	
Min clock pulse width	t _W	_	10	_	20	100	ns
Will Glock paloe width	LVV		15	_	15	80	110
			5		40	200	
Min pulse width	twH		10		20	80	ns
(STROBE)	WH		15		15	70	113
			5	1.25	6	70	
Max clock frequency	f _{CL}	_	10	2.50	12		MHz
max clock frequettey	ICL	_	15	3.00	16		IVII IZ
			5		0	120	
Min set-up time	tou		10	_	0	55	ns
(DATA-CLOCK)	tsu	_	15		0	35	113
Min hold time	4		5	_	10	40	20
(DATA-CLOCK)	tH	_	10		10	20	ns
			15	_	5	15	
Min set-up time			5	_	90	200	
(CLOCK-STROBE)	tsu	_	10		40	100	ns
			15	_	30	80	

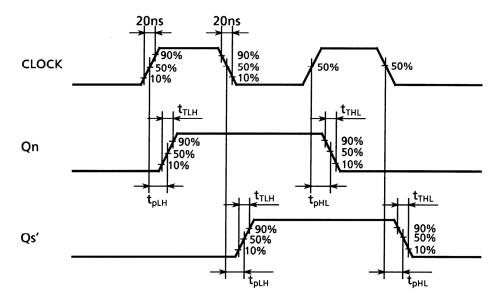
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Characteristics	Symbol	Test Condition	V _{DD} (V)	Min	Тур.	Max	Unit
Min hold time (CLOCK-STROBE)	t _H	_	5 10 15	— — —	— — —	0 0 0	ns
Max clock input rise time Max clock input fall time	t _{rCL}	_	5 10 15		No limit		μѕ
Input capacitance	C _{IN}	_		_	5	7.5	pF

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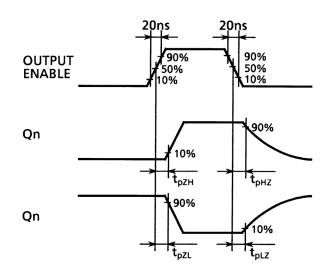
Waveforms for Measurement of Dynamic Characteristics

Waveform 1

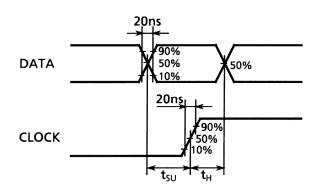


Waveform 2

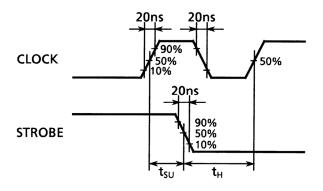
Waveform 3



Waveform 4

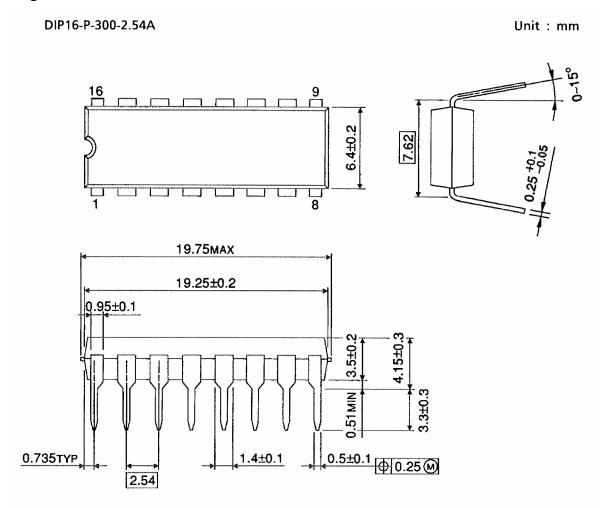


Waveform 5





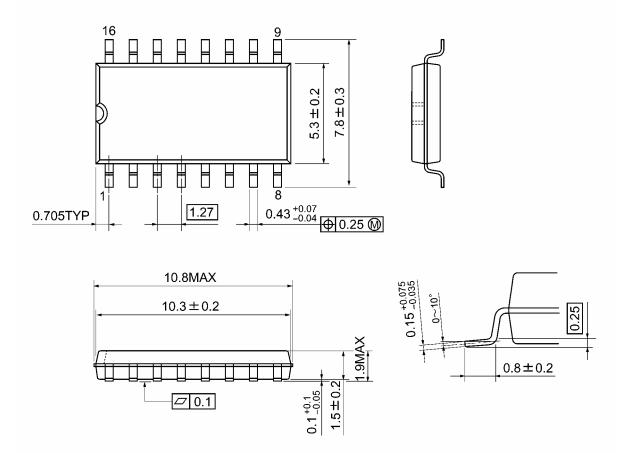
Package Dimensions



Weight: 1.00 g (typ.)

Package Dimensions

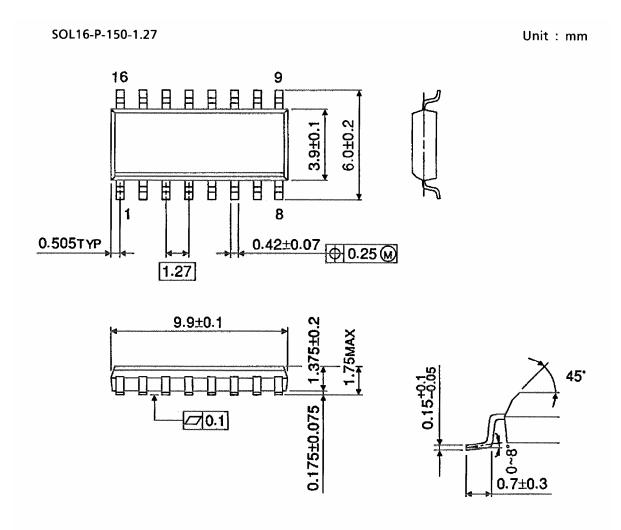
SOP16-P-300-1.27A Unit: mm



Weight: 0.18 g (typ.)



Package Dimensions (Note)



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

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20070701-EN GENERAL

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